REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Status of Claims:

Claim 2 is currently being cancelled.

Claims 1, 3-12 and 15-19 are currently being amended.

Claim 24 is currently being added.

This amendment and reply adds, cancels and amends claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claims remain under examination in the application, is presented, with an appropriate defined status identifier.

After adding, canceling and amending the claims as set forth above, claims 1, 3-12 and 15-24 are now pending in this application.

Claim Rejections – 35 U.S.C. § 112, 2nd Paragraph:

In the Office Action, claim 11 was rejected under 35 U.S.C. § 112, 2nd Paragraph, as being indefinite, because the Office Action asserts that the term "containing . . . means no other elements can be in the insulating film other than silicon and nitrogen." In reply, this interpretation of the term "containing" is incorrect, since it is an inclusive term and not an exclusive term. In any event, "containing" has been replaced with "that includes" in claim 10 (as well as the other claims where this term was used), to make it clear that other elements besides silicon and nitrogen can be in the insulating film. Accordingly, dependent claim 11 is not inconsistent with the recitations in claim 10.

Claim Rejections – 35 U.S.C. § 102(e):

In the Office Action, claims 1-3, 5, 6, 8, 10-12, 15 and 17 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,867,078 to Green et al. Applicants are filing a verified English language translation of the priority document, Japanese Patent Application 2002-364405. Accordingly, Applicants have perfected their priority date of December 16, 2002, which antedates the November 19, 2003 filing date of Green et al.

As such, this rejection has been overcome.

Claim Rejections – 35 U.S.C. § 103(a):

In the Office Action, claims 1-4, 8-12, 18, 22 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Publication No. 2001/0015446 to Inoue in view of U.S. Patent Publication No. 2002/0079525 to Mayuzumi; claims 5, 6 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inoue in view of Mayuzumi and further in view of U.S. Patent No. 6,483,135 to Mizuta et al.; claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Inoue in view of Mayuzumi and further in view of U.S. Patent Publication No. 2003/0020092 to Parikh et al.; claims 16 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inoue in view of Mayuzumi and Mizuta et al., and further in view of U.S. Patent Publication No. 2001-0017370 to Sheppard et al.; and claims 19-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inoue in view of Mayuzumi and further in view of U.S. Patent Publication No. 2002/0043697 to Hirokawa. These rejections are traversed with respect to the presently pending claims under rejection, for at least the reasons given below.

In its rejection of claim 1, the Office Action asserts that Mayuzumi teaches an insulating film 9 that is a multilayered film including a first insulating film 3 and a second insulating film (2 or 7).

However, the insulating film 9 of Mayuzumi is a side wall. A side wall is a structure specific to a MOS transistor that has an LDD (Lightly Doped Region) structure, and it can not be adapted to an HJFET of Inoue.

In Mayuzumi, the MOS transistor that has an LDD (Lightly Doped Region) structure is manufactured as follows.

A low concentration diffusion layer 10a (which makes a source/drain region) is formed at the surface of the substrate 1 beneath the insulating film 2. Subsequently, a high concentration diffusion layer 10b (which makes a source/drain region) is formed at the exposed surface of the substrate 1 by ion implantation using the side wall as a mask (please see Fig. 8 and [0050]). Therefore, it can be understood that a side wall is a mask to form a high concentration diffusion layer.

Therefore, it is not possible to use a side wall in the HJFET of Inoue, because the HJFET of Inoue does not have a high concentration diffusion layer.

The inventors of the present application found that it is difficult to maintain the compatibility between the collapse and the gate breakdown voltage in GaN semiconductor FET, and they came up with a GaN semiconductor FET which is excellent for the balance between the collapse and the gate breakdown voltage by using the field-plate and using the insulating film that has specific layer structure. The above problem does not occur in Mayuzumi, because the transistor of Mayuzumi is a MOSFET. In Mayuzumi, the side wall having two insulating films is just used for preventing itself from etching when a contact hole is etched, as explained in paragraph 0016 of Mayuzumi.

Furthermore, Inoue does not teach or suggest that it is difficult to maintain the compatibility between the collapse and the gate breakdown voltage in GaN semiconductor FET.

As recited in presently pending independent claim 1 (which now includes the features of claim 2, now canceled), the second insulating film having a dielectric constant lower than that of the first insulating film is laminated on the first insulating film being made of a compound containing silicon and nitrogen as constituent elements. On the contrary, Mayuzumi discloses that a SiN or SiON film 3 is laminated on a SiO_2 film 2. In other words, Mayuzumi discloses that a first insulating film being made of a compound containing silicon and nitrogen as constituent elements is laminated on a second insulating film having a dielectric constant lower than that of the first insulating film. When the first insulating film is laminated on the second insulating film, it is difficult to lessen a probability of collapse. Note that claim 1 recites that the second insulating film is laminated on the first insulating film, and not the other way around.

Thus, since Mayuzumi cannot be combined with Inoue for the reasons discussed in detail above (MOS transistor versus HJFET), and since even if such a combination could be made for argument sake it would not teach or suggest all of the features recited in claim 1, that claim patentably distinguishes over the cited art of record.

With respect to the other independent claims under rejection, since Mayuzumi cannot be combined with Inoue for the reasons discussed in detail above (MOS transistor versus HJFET), those claims also patentably distinguish over the cited art of record.

New Claim:

New claim 24 has been added to recite features seen in Figure 6 of the drawings, in which a double-stepped structure of an insulating film 22 can clearly be seen in that figure.

Conclusion:

Since all of the issues raised in the Office Action have been addressed in this Amendment and Reply, Applicants believe that the present application is now in condition for allowance, and an early indication of allowance is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing or a credit card payment form being unsigned, providing incorrect information resulting in a rejected credit card transaction, or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicants hereby petition for such extension under 37 C.F.R. §1.136 and authorize payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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